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To: Inez McMillan
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Group Art Unit 2100

Fax No.: 703-872-9306

From: Holly N. Moore

Your Ref.: U.S. Patent Application No. 09/424,667 Our Ref.: 104822

Number of Pages Sent (Including cover sheet): 32

Prepared By: aj

Comments:

Sent by: ajl

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Makoto KUDO et al.

Group Art Unit: 2184

Application No.: 09/424,667

Examiner: B. Bonzo

Filed: March 15, 2000

Docket No.: 104822

For: MICROCOMPUTER, ELECTRONIC EQUIPMENT AND DEBUGGING SYSTEM

STATUS INQUIRY LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants filed an Amendment with an Amendment Transmittal and copy of the November 29, 1999 Form PTO-1449 in the U.S. Patent and Trademark Office Mailroom on October 21, 2003. Additionally, Applicants filed a Supplemental Amendment in the U.S. Patent and Trademark Office Mailroom on December 1, 2003.

A personal interview with Examiner Bonzo was conducted on October 30, 2003 where the October 21, 2003 Amendment was discussed. Thereafter, a Supplemental Amendment was filed on December 1, 2003.

After numerous telephone conversations with Examiner Bonzo, he indicated that he has not yet received the December 1 submission for review. Further, Examiner Bonzo indicated that the application file is currently unavailable. Thus, attached is a copy of the November 29, 1999 Form PTO-1449, October 21, 2003 Amendment, Amendment Transmittal, December 1, 2003 Supplemental Amendment, and copy of the stamped U.S. PTO acknowledgement of receipt as filed in the PTO mailroom on October 21, 2003 and

PAGE 2/32 * RCVD AT 4/30/2004 11:33:13 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:7038362787 * DURATION (mm-ss):10-18

December 1, 2003. Also attached is a copy of Check No. 147550 which was submitted with the October 21, 2003 Amendment.

Please telephone our firm's Patent Application Filing Department at 703-836-6400 with the status of the above-identified patent application, including an indication as to when the next communication can be expected.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Holly N. Moore
Registration No. 50,212

JAO:HNM/al

Attachments:
- Copy of Check No. 147550
- PTO Date-Stamped Receipt of December 1, 2003
- PTO Date-Stamped Receipt of October 21, 2003
- Copy of December 1, 2003 Supplemental Amendment
- Copy of October 21, 2003 Amendment
- Copy of October 21, 2003 Amendment Transmittal
- Copy of November 29, 1999 PTO-1449

Date: April 30, 2004

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SUPPLEMENTAL AMENDMENT

Name of Applicant: Makoto KUDO et al.

Serial No.: 09/424,667

Atty. File No.: 104822

Title (New Cases):

Sender's Initials: JAO:HNS/cfr

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AMENDMENT TRANSMITTAL W/CK# 147550 FOR $144.00; AMENDMENT W/COPIES OF 11/29/1999 FORM PTO-1449 AND COPY OF STAMPED PTO ACKNOWLEDGEMENT OF RECEIPT

Name of Applicant: Makoto KUDO et al.

Serial No.: 09/424,667

Atty. File No.: 104822

Title (New Cases):

Sender's Initials: JAO:HNS/cfr

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PATENT APPLICATION

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Makoto KUDO et al.

Application No.: 09/424,667

Filed: March 15, 2000

Group Art Unit: 2184

Examiner: B. Bonzo

Docket No.: 104822

For: MICROCOMPUTER, ELECTRONIC EQUIPMENT AND DEBUGGING SYSTEM

SUPPLEMENTAL AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Further to the Amendment filed October 21, 203 and the October 30, 2003 personal interview, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A microcomputer having an on-chip debugging function, comprising:

a central processing unit for executing instructions; and

a first monitor section which performs data transfer to and from a second monitor section, determines a primitive command to be executed based on the receive data from said second monitor section, and performs processing for execution of the determined primitive command, said second monitor section being provided outside said microcomputer and performing a processing to convert a debugging command into at least one primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section, said first monitor section includes a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization, and a circuit for sending and receiving data based on said first sampling clock, said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

2. (Previously Presented) The microcomputer according to claim 1, said primitive command includes a command for starting an execution of a user program, a command for writing data to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.

3. (Previously Presented) The microcomputer according to claim 1, the first monitor section includes a control register used for execution of instructions in said central

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processing unit and having an address thereof allocated on a memory map in a debugging mode.

4. (Previously Presented) The microcomputer according to claim 2, the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on the memory map in the debugging mode.

5. (Previously Presented) The microcomputer according to claim 1, the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

6. (Previously Presented) The microcomputer according to claim 2, the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on the memory map in the debugging mode.

7. (Previously Presented) The microcomputer according to claim 1, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

8. (Previously Presented) The microcomputer according to claim 2, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a

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processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

9. (Previously Presented) The microcomputer according to claim 1, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

10. (Previously Presented) The microcomputer according to claim 2, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

11. (Previously Presented) The microcomputer according to claim 1, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

12. (Previously Presented) The microcomputer according to claim 2, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

13. (Previously Presented)The microcomputer according to claim 1, wherein a monitor program for executing a processing of said first monitor section is stored in a ROM.

14. (Previously Presented) The microcomputer according to claim 2, wherein a monitor program for executing a processing of said first monitor section is stored in a ROM.

15. (Cancelled).

16. (Previously Presented) The microcomputer according to claim 2, said first monitor section includes:

a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and

wherein said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

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17. (Previously Presented) The microcomputer according to claim 1, said first monitor section includes a monitor RAM which is readable and writable, and when a break of an execution of an user program occurs and a mode is shifted to a debugging mode, said first monitor section saves a program counter value of said central processing unit and contents of an internal register into said monitor RAM.

18. (Previously Presented) The microcomputer according to claim 2, said first monitor section includes a monitor RAM which is readable and writable, and when a break of an execution of an user program occurs and a mode is shifted to a debugging mode, said first monitor section saves a program counter value of said central processing unit and contents of an internal register into said monitor RAM.

19. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 1;

an input source of data to be processed by said microcomputer;

and

an output device for outputting data processed by said microcomputer.

20. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 2;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

21. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 3;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

22. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 5;

an input source of data to be processed by said microcomputer; and

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an output device for outputting data processed by said microcomputer.

23. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 7;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

24. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 9;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

25. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 11;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

26. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 13;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

27. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to ~~claim 15~~claim 1;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

28. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 17;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

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29. (Currently Amended) A debugging system for a target system including a microcomputer, said debugging system comprising:

a second monitor section which performs processing for converting a debugging command issued by a host system into at least one primitive command; and

a first monitor section which performs data transfer to and from said second monitor section, determines a primitive command to be executed based on the receive data from said second monitor section, and performs processing for execution of the determined primitive command, wherein the second monitor section converts the debugging command into the primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section, said first monitor section includes a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization, and a circuit for sending and receiving data based on said first sampling clock, said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

30. (Previously Presented) The debugging system according to claim 29, said primitive command includes a command for starting an execution of a user program, a command for writing data to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.

31. (Previously Presented) The debugging system according to claim 29, the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on a memory map in a debugging mode.

32. (Previously Presented) The debugging system according to claim 29, the first monitor section includes a monitor RAM into which contents of an internal register of said

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central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

33. (Previously Presented) The debugging system according to claim 29, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

34. (Previously Presented) The debugging system according to claim 29, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

35. (Previously Presented) The debugging system according to claim 29, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

36. (Previously Presented) The debugging system according to claim 29, wherein a monitor program for executing a processing of said first monitor section is stored in a ROM.

37. (Previously Presented) The debugging system according to claim 29, said first monitor section includes:

a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and

wherein said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

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REMARKS

Claims 1-37 are pending in this application. By this Amendment, claims 1, 27 and 29 are amended. Reconsideration based on the above amendments and following remarks is respectfully requested.

Applicants gratefully appreciate the courtesies extended to Applicants' representative by the Examiner during the personal interview.

I. The Claims Satisfy All Formal Requirements

Although not objected to by the Examiner, claim 27 has been amended to correct informalities. No new matter has been added.

II. The Claims Define Allowable Subject Matter

The Office Action rejects claims 1-12, 17-25, 28 and 29 under 35 U.S.C. §102(e) as unpatentable over U.S. Patent No. 6,314,530 to Mann (hereinafter "Mann"); and claims 13, 14 and 26 under 35 U.S.C. §103(a) as unpatentable over Mann. These rejections are respectfully traversed.

The Office Action indicates that claim 15 contains allowable subject matter. Amended claims 1 and 29 incorporate the limitation of cancelled claim 15. No new matter has been added

Claims 1 and 29, as amended, distinguish over the prior art in that they include a first monitor section that includes a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization, and a circuit for sending and receiving data based on the first sampling clock, and the first monitor section supplies the first clock to the second monitor section as a signal for causing a second frequency division circuit included in the second monitor section to generate a second sampling clock.

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For at least these reasons, it is respectfully submitted that claims 1 and 29 are distinguishable over the applied art. Claims 2-14, 16-28, and 30-37, which depend from claims 1 and 29, are likewise distinguishable over the applied art for at least the reasons discussed as well as for the additional features they recite. Withdrawal of the rejections under 35 U.S.C. §102(e) and 35 U.S.C. §103(a) is respectfully requested.

III. Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-14 and 16-37 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Holly N. Sy
Registration No. 50,212

JAO:HNS/cfr

Date: December 1, 2003

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Makoto KUDO et al.

Application No.: 09/424,667

Filed: March 15, 2000

Group Art Unit: 2184

Examiner: B. Bonzo

Docket No.: 104822

For: MICROCOMPUTER, ELECTRONIC EQUIPMENT AND DEBUGGING SYSTEM

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the July 21, 2003 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A microcomputer having an on-chip debugging function, comprising:

a central processing unit for executing instructions; and

a first monitor ~~means for performing~~ section which performs data transfer to and from a second monitor ~~means~~ section, ~~determining~~ determines a primitive command to be executed based on the receive data from said second monitor ~~means~~ section, and ~~performing~~ performs processing for execution of the determined primitive command, said second monitor ~~means~~ section being provided outside said microcomputer and ~~for~~ performing a processing to convert a debugging command into at least one primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section.

2. (Currently Amended) The microcomputer according to claim 1, ~~wherein~~ said primitive command includes a command for starting an execution of a user program, a command for writing data to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.

3. (Currently Amended) The microcomputer according to claim 1, ~~further comprising~~ the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on a memory map in a debugging mode.

4. (Currently Amended) The microcomputer according to claim 2, ~~further comprising~~ the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on the memory map in the debugging mode.

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5. (Currently Amended) The microcomputer according to claim 1, ~~further comprising~~ the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

6. (Currently Amended) The microcomputer according to claim 2, ~~further comprising~~ the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on the memory map in the debugging mode.

7. (Currently Amended) The microcomputer according to claim 1, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor ~~means~~ section,

———wherein, on condition that said first monitor ~~means~~ section being a slave has received data from said second monitor ~~means~~ section being a master, said first monitor ~~means~~ section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor ~~means~~ section.

8. (Currently Amended) The microcomputer according to claim 2, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor ~~means~~ section,

———wherein, on condition that said first monitor ~~means~~ section being a slave has received data from said second monitor ~~means~~ section being a master, said first monitor ~~means~~ section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor ~~means~~ section.

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9. (Currently Amended) The microcomputer according to claim 1, ~~wherein~~ the data received from said second monitor ~~means~~ section includes an identification data of the primitive command to be executed by said first monitor ~~means~~ section.

10. (Currently Amended) The microcomputer according to claim 2, ~~wherein~~ the data received from said second monitor ~~means~~ section includes an identification data of the primitive command to be executed by said first monitor ~~means~~ section.

11. (Currently Amended) The microcomputer according to claim 1, wherein said first monitor ~~means~~ section transfers fixed-length data to and from said second monitor ~~means~~ section.

12. (Currently Amended) The microcomputer according to claim 2, wherein said first monitor ~~means~~ section transfers fixed-length data to and from said second monitor ~~means~~ section.

13. (Currently Amended)The microcomputer according to claim 1, wherein a monitor program for executing a processing of said first monitor ~~means~~ section is stored in a ROM.

14. (Currently Amended) The microcomputer according to claim 2, wherein a monitor program for executing a processing of said first monitor ~~means~~ section is stored in a ROM.

15. (Currently Amended) The microcomputer according to claim 1, ~~wherein~~ said first monitor ~~means comprises~~ section includes:

a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and

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wherein said first monitor ~~means~~ section supplies said first clock to said second monitor ~~means~~ section as a signal for causing a second frequency division circuit included in said second monitor ~~means~~ section to generate a second sampling clock.

16. (Currently Amended) The microcomputer according to claim 2, ~~wherein~~ said first monitor ~~means comprises~~ section includes:

a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and

wherein said first monitor ~~means~~ section supplies said first clock to said second monitor ~~means~~ section as a signal for causing a second frequency division circuit included in said second monitor ~~means~~ section to generate a second sampling clock.

17. (Currently Amended) The microcomputer according to claim 1, ~~wherein:~~

~~—~~said first monitor ~~means~~ section includes a monitor RAM which is readable and writable, and

~~—~~when a break of an execution of an user program occurs and a mode is shifted to a debugging mode, said first monitor ~~means~~ section saves a program counter value of said central processing unit and contents of an internal register into said monitor RAM.

18. (Currently Amended) The microcomputer according to claim 2, ~~wherein:~~ said first monitor ~~means~~ section includes a monitor RAM which is readable and writable, and

~~—~~when a break of an execution of an user program occurs and a mode is shifted to a debugging mode, said first monitor ~~means~~ section saves a program counter value of said central processing unit and contents of an internal register into said monitor RAM.

19. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim 1;

an input source of data to be processed by said microcomputer;

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and

an output device for outputting data processed by said microcomputer.

20. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim 2;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

21. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim 3;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

22. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim 5;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

23. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim 7;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

24. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim 9;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

25. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim 11;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

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26. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim 13;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

27. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim 15;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

28. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim 17;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

29. (Currently Amended) A debugging system for a target system including a microcomputer, said debugging system comprising:

a second monitor ~~means for performing~~ section which performs processing for converting a debugging command issued by a host system into at least one primitive command; and

a first monitor ~~means for performing~~section which performs data transfer to and from said second monitor ~~means~~section, ~~determining~~determines a primitive command to be executed based on the receive data from said second monitor ~~means~~section, and ~~performing~~performs processing for execution of the determined primitive command, wherein the second monitor section converts the debugging command into the primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section.

30. (New) The debugging system according to claim 29, said primitive command includes a command for starting an execution of a user program, a command for writing data

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to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.

31. (New) The debugging system according to claim 29, the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on a memory map in a debugging mode.

32. (New) The debugging system according to claim 29, the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

33. (New) The debugging system according to claim 29, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

34. (New) The debugging system according to claim 29, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

35. (New) The debugging system according to claim 29, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

36. (New) The debugging system according to claim 29, wherein a monitor program for executing a processing of said first monitor section is stored in a ROM.

37. (New) The debugging system according to claim 29, said first monitor section includes:

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a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and

wherein said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

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REMARKS

Claims 1-37 are pending in this application. By this Amendment, claims 1-29 are amended, and claims 30-37 are added. Reconsideration based on the above amendments and following remarks is respectfully requested.

Applicants gratefully acknowledge that the Office Action indicates that claims 15, 16 and 27 include allowable subject matter.

I. Information Disclosure Statement

An Information Disclosure Statement with Form PTO-1449 was filed in the above-captioned patent application on March 15, 2000. Applicants have not yet received from the Examiner a copy of the PTO-1449 initialed to acknowledge the fact that the Examiner has considered disclosed information. The Examiner is requested to initial and return to the undersigned a copy of the Form PTO-1449. For the convenience of the Examiner, a copy of that form is attached. Applicants respectfully request that the Examiner consider and return the original Form PTO-1449 with the next Office Action.

II. Notice Regarding Fees

The Office Action indicates that claims 19-28 have been interpreted by the Examiner as being in independent form. Further, the Office Action indicates that the Examiner views the referencing of prior claims as a shorthand form which does not render the claims in dependent form. Thus, the Office Action asserts that claims 19-28 are being examined and fully treated as independent claims, wherein the balance of the fees shall be charged to the Applicants at the time of mailing of the Office Action. However, Applicants respectfully submit that this interpretation is improper.

37 C.F.R. §1.75(c) states the following:

> One or more claims may be presented in dependent form, referring back to and further limiting another claim or claims in the same application.

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> Claims in dependent form shall be construed to include all the limitations of the claim incorporated by reference into the dependent form.

Since claims 19-28 include all of the limitations of the claim incorporated by reference into the dependent claim, claims 19-28 are in proper dependent form. Therefore, Applicants respectfully submit that claims 19-28 must be examined as independent claims for prosecution on the merits and fee purposes.

III. The Claims Satisfy All Formal Requirements

Although not objected to by the Examiner, claims 1-29 have been amended to correct informalities. No new matter has been added.

IV. The Claims Define Allowable Subject Matter

The Office Action rejects claims 1-12, 17-25, 28 and 29 under 35 U.S.C. §102(e) as unpatentable over U.S. Patent No. 6,314,530 to Mann (hereinafter "Mann"); and claims 13, 14 and 26 under 35 U.S.C. §103(a) as unpatentable over Mann. These rejections are respectfully traversed.

Mann does not disclose "a first monitor section which performs data transfer to and from a second monitor section, determines a primitive command to be executed based on the received data from said second monitor section, and performs processing for execution of the determined primitive command," and a second monitor section that converts "the debugging command into at least one primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section," as recited in claims 1 and 29.

The Office Action asserts that a debug port 100 in Fig. 1 of Mann is equivalent to a first monitor section as recited in claims 1 and 29. However, as shown in Fig. 2 of Mann, the debut port 100 in Fig. 1 is a trace circuit including a trace cache 200, a trace debug interface logic 216, trace control circuitry 218, and a trace pad interface port 220 for tracing the state of the processor core. See column 6, 12 - column 7, line 26.

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Mann discloses a target system T having an embedded processor device 102 and a system memory 106. The embedded processor device 102 includes a processor core 104 and a debug port 100. See col. 5, lines 42-47. The prodessor device 102, as shown in Fig. 2, includes trace control circuitry 218 and trace cache 200 that provides trace information for reconstructing instruction execution flow in the processor core 104. Further, the processor device 102 includes trace pad interface port 220 capable of providing trace data while the processor core 104 is executing instructions. See col. 6, lines 12-29. An enhanced embodiment of debug port 100 adds additional signals to allow for pinpoint accuracy and extra functionality, and improve communications speeds for debug port 100.

Before debug information is communicated via the debug port 100 using only conventional JTAG signals, the port 100 is enabled while writing the public JTAG instruction DEBUG into a JTAG instruction register contained within the TAP controller 204. Col. 7, lines 15-19. The JTAG TAP controller 204 accepts standard JTAG zero data and control. When a debug instruction has been written to the JTAG instruction register, serial debug shifter 212 is connected to the JTAG test data input signal TEI and test data output signal TDO, such that commands and data can then be loaded into and read from the debug registers 210.

Although Mann discloses trace control circuitry 218 and trace cache 200 providing trace information for a reconstructing instruction execution flow in processor core 104, they are part of the trace circuit and not a first monitor section, as recited in claims 1 and 29. Thus, trace control circuitry 218 and trace cache 200 cannot be considered as equivalent to the first monitor section, as recited in claims 1 and 29.

Additionally, Mann does not disclose that debug port 100 converts a debugging command into at least one primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section. Mann is

completely devoid of disclosure that a second monitor section converts a complicated debugging command into a simple and primitive command..

Furthermore, Mann does not disclose that the first monitor section receives data from the second monitor section, and determines a primitive command to be executed based on the received data from the second monitor section, as recited in claims 1 and 29. See page 10, line 1 to page 11, line 16, and page 11, line 17 to page 14, line 5, and Figs. 2 to 4 of the present application. For example, in Fig. 2 of Mann, the interface port 220 does not receive data. Instead, the interface port 220 merely outputs a trace data (TBUS [19:0]) of a processor core, because the interface port 220 is an interface for a trace circuit. See Fig. 2 and column 6, lines 15-27.

Since the configuration of Mann does not include a second monitor section as recited in claims 1 and 29, an increase of processing in a target system. Thus, a complicated circuit, such as a processor device 102 of Mann, is necessitated to realize a debugging function in a hardware.

Also, Mann does not disclose that primitive command includes a command for starting an execution of a user program, a command for writing data to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map, as recited in claim 2. Additionally, Mann does not disclose that the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on a memory map in a debugging mode, as recited in claims 3 and 4. Finally, Mann does not disclose that the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode, as recited in claims 5 and 6.

For at least these reasons, it is respectfully submitted that claims 1 and 29 are distinguishable over the applied art. Claims 2-28 and 30-37, which depend from claims 1 and

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29, are likewise distinguishable over the applied art for at least the reasons discussed as well as for the additional features they recite. Withdrawal of the rejections under 35 U.S.C. §102(e) and 35 U.S.C. §103(a) is respectfully requested.

V. Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-30 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Holly N. Sy
Registration No. 50,212

JAO:HNS/cfr

Attachments:
Form PTO-1449 (filed November 29, 1999)
Stamped PTO acknowledgement of receipt

Date: October 21, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
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PATENT APPLICATION

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Attorney Docket No.: 104822

AMENDMENT TRANSMITTAL

In re the Application of

Makoto KUDO et al.

Application No.: 09/424,667

Filed: March 15, 2000

Group Art Unit: 2184

Examiner: B. Bonzo

For: MICROCOMPUTER, ELECTRONIC EQUIPMENT AND DEBUGGING SYSTEM

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Amendment in the above-identified application.

☐ Entitlement to small entity status is hereby asserted.

☐ Small entity status of this application has been established.

The filing fee has been calculated as shown below:

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT	(Column 2) HIGHEST NO. PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADD'L FEE	OR	OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY ADD'L FEE
TOTAL CLAIMS	*37 MINUS	**29	=8	x 9	$		x 18	$ 144
INDEP CLAIMS	*2 MINUS	***3	=0	x 43	$		x 86	$ 0
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+145	$	OR	+290	$
					$			$ 144

* If the entry in Column 1 is less than the entry in Column 2, write "0" in Column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.

The "Highest Number Previously Paid For" in this space (Total or Independent) is the highest number found from the equivalent box in Column 1 of a prior Amendment or the number of claims originally filed.

☒ Check No. 147550 in the amount of $144.00 is attached. The Commissioner is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 15-0461. Two duplicate copies of this sheet are attached.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Holly N. Sy
Registration No. 50,212

JAO:HNS/cfr

Date: October 21, 2003

Sheet 1 of 1

Form PTO-1449 (REV. 8-83)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 104822	New U.S. National Stage of PCT/JP99/01655
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT(S) Makoto KUDO and Yoichi HIJIKATA	
		FILING DATE November 29, 1999	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	1	60-72034	04/1985	Japan		
	2	8-221297	08/1996	Japan		
	3	1-286030	11/1989	Japan		
	4	64-3745	01/1989	Japan		
	5	63-303437	12/1988	Japan		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER			DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

November 29, 1999